## REMARKS

Claims 1-39 are pending in this application.

Claims 4-23 have been previously withdrawn due to a restriction requirement.

Claims 1-2, 24-29 and 33-39 have been rejected.

Claims 3 and 30-32 have been objected to.

Claim 33 has been amended.

Claims 1-39, as amended, remain pending in this application.

Reconsideration of Claims 1-39, as amended, is respectfully requested.

## I. ALLOWABLE SUBJECT MATTER

The Examiner stated that Claim 3 and Claims 30-32 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. (November 20, 2007 Office Action, Page 4, Paragraph 6). The Applicants thank the Examiner for the indication that Claim 3 and Claims 30-32 would be allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Because the Applicants believe that the remaining claims in this application are allowable, the Applicants have not rewritten Claim 3 and Claims 30-32 in independent form at this time.

The Examiner also stated that Claims 37-39 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112, second paragraph, and to include all of the limitations of the base claim and any intervening claims. (November 20, 2007 Office Action, Page 5, Paragraph 7). As described more fully below, the Applicants have now amended Claim 33 to overcome the indefiniteness rejections under 35 U.S.C. § 112, second paragraph. The Applicants respectfully submit that Claims 37-39 are now in condition for allowance.

## II. CLAIM REJECTIONS UNDER 35 U.S.C. § 112

The Examiner stated that Claims 33-39 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. (November 20, 2007 Office Action, Page 2, Paragraph 2, Lines 1-3). The Examiner stated that Claim 33 is misdescriptive of the invention because the synchronized oscillator of the invention comprises an astable multivibrator. The Examiner also stated that Claims 34-39 are indefinite because of the technical deficiencies of Claim 33. (November 20, 2007 Office Action, Page 2, Paragraph 2, Lines 4-8).

In response, the Applicants have amended Claim 33 to claim a synchronized oscillator that comprises an astable multivibrator. The Applicants respectfully submit that the amendment of Claim 33 overcomes the indefiniteness rejections and that Claims 33-39, as amended, are now in condition for allowance.

## III. CLAIM REJECTIONS UNDER 35 U.S.C. § 102

Claim 1 and Claim 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,782,246 to Kuroyanagi et al. (hereafter "*Kuroyanagi*").

Claims 1-2, 24-29 and 33-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,585 to Dai et al. (hereafter "*Dai*").

The Applicants respectfully traverse these rejections for the reasons set forth below.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Examiner stated that the circuit shown in Figure 1 of the *Kuroyanagi* reference anticipates the Applicants' invention as claimed in Claim 1 and in Claim 24. (November 20, 2007 Office Action, Page 2, Lines 22-23). The Applicants respectfully point out that the *Kuroyanagi* reference fails to anticipate a "synchronized oscillator" of the type disclosed and claimed by the Applicants. The *Kuroyanagi* reference fails to anticipate a "synchronized oscillator" having a "variable free-running oscillation frequency" controlled by a "control signal," where the "control signal" controls a "phase-shift" of an "output signal" with respect to an "input signal."

The *Kuroyanagi* reference discloses the use of differential amplifier means and variable current means. The circuit elements that are shown in Figure 1 of the *Kuroyanagi* reference do not form or operate a synchronized oscillator. The *Kuroyanagi* reference states that the phase shift circuit 16 functions as a high-pass filter and a low-pass filter in combination. (*Kuroyanagi*, Column 3, Lines 37-40). The high-pass filter and low-pass filter of the *Kuroyanagi* device do not operate as a synchronized oscillator. Therefore, *Kuroyanagi* device does not anticipate the Applicants' invention as claimed in Claim 1 or in Claim 24.

The Applicants respectfully traverse the Examiner's assertion that the elements 101-104 and 150-152 of *Kuroyanagi* constitute a synchronized oscillator. The arrangement of the *Kuroyanagi* reference is based on a differential amplifier. It is designed to provide phase difference between input and output signals wherein the amount of phase shift can be controlled to be fixed to a pre-determined value. The Applicants respectfully submit that there is nothing in the *Kuroyanagi* reference to support the Examiner's assertion that the above mentioned elements constitute a synchronized oscillator.

An oscillator is a circuit that generates an oscillating signal on its own and is not a circuit that reproduces oscillations of an oscillating signal received from the exterior. The circuit 16 that is shown in Figure 1 of the *Kuroyanagi* reference cannot generate oscillations 25 at the output 25 in the absence of an oscillating signal that is fed in at the input 23. The November 20, 2007 Office Action fails to explain which elements of circuit 16 comprise an oscillator.

A voltage controlled oscillator is disclosed in the circuit shown in Figure 4 and is described in the corresponding portion of the *Kuroyanagi* reference. (Kuroyanagi, Column 5, Line 58 to Column 6, Line 29). However, the voltage controlled oscillator comprises the variable phase shifter 16 and not the opposite. The Applicants' invention relates to a phase shifting circuit that comprises a synchronized oscillator. Therefore, prior art references that show oscillators comprising phase shifting circuits are irrelevant to the question of patentability.

In addition, unlike the Applicants' invention, the control signal in the *Kuroyanagi* device originates from a phase detector 15 within the *Kuroyanagi* device. As claimed in Claim 1 of the *Kuroyanagi* patent, the phase detector 15 is part of the *Kuroyanagi* device. The phase detector 15 compares the phase of the input signal 23 and the phase of the output signal 25 and provides a resulting control signal to input 24. The control signal in the Applicants' invention does not originate in the Applicants' variable phase shifting circuit 40.

For these reasons, the elements of the *Kuroyanagi* reference do not anticipate the Applicants' invention as claimed in Claim 1 and Claim 24. Accordingly, the Applicants respectfully request withdrawal of the §102 rejections and full allowance of Claim 1 and Claim 24.

The Examiner also stated that the circuit shown in Figure 3 of the *Dai* reference anticipates the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. (November 20, 2007 Office Action, Page 3, Lines 17-18). The Applicants respectfully point out that the circuit that is shown in Figure 3 of the *Dai* reference is a delay stage 32 for a ring-type voltage controlled oscillator 30. The delay stage 32 comprises inverters (33 and 34), a memory circuit (35) and tuning

circuitry (transistors M1, M4, M7 and M10). The transistors of the tuning circuitry function as variable resistors to tune the amount of delay of the delay stage 32, and hence the frequency of the voltage controlled oscillator 30. (*Dai*, Column 4, Lines 23-28). The frequency (not the phase) is tuned. Therefore, the *Dai* reference does not show a phase shifter circuit.

The Examiner stated that the cross coupled transistors M5 and M6 in the *Dai* reference form a synchronized oscillator that maintain an oscillation of the output signal. (November 20, 2007 Office Action, Page 3, Lines 23-24). The Applicants respectfully traverse this assertion of the Examiner. The *Dai* reference states that "The memory element 35 in the configuration shown in FIG. 3 operates to prevent the outputs of inverters 33 and 34 from switching states when they otherwise would switch. In other words, memory element 35 causes switching to be delayed." (*Dai*, Column 5, Lines 58-62). The Applicants respectfully submit that the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

The cross coupled transistors M5 and M6 constitute a very stable circuit 35 (as it must be for a memory, namely a latch). The electrical state of this memory circuit 35 can only be changed by applying a switching signal at the input. In the absence of such switching signal input to the cross coupled transistors M5 and M6, there will be no variation at the output. Therefore, the memory circuit 35 can not be equivalent to an oscillator circuit.

Furthermore, the *Dai* reference states that "In accordance with the invention, the strength of inverters 33 and 34 is variable and dependent upon the control voltage received by the tuning transistors M1, M4, M7 and M10, whereas the strength of the memory element 35

remains relatively constant as it is tied, in the case of FIG. 3, to the power supply voltage $V_{DD}$. (*Dai*, Column 5, Line 67 to Column 6, Line 6) (Emphasis added). Because the strength of the memory element 35 remains relatively constant, the memory element 35 is not a synchronized oscillator that has a variable free-running oscillation frequency that is controlled by a control signal. There is no control signal in the *Dai* reference that controls the relatively constant memory element 35. This is because the cross coupled transistors M5 and M6 operate as a memory element 35 and not as a synchronized oscillator.

For these reasons, the elements of the *Dai* reference do not anticipate the Applicants' invention as claimed in Claims 1-2, 24-29 and 33-36. Accordingly, the Applicants respectfully request withdrawal of the §102 rejections and full allowance of Claims 1-2, 24-29 and 33-36.

## IV. CONCLUSION

For the foregoing reasons, the Applicants respectfully request full allowance of all pending claims and that this application be passed to issuance.

The Applicants' attorney has made the amendments and arguments set forth above in order to place this application in condition for allowance. In the alternative, the Applicants' attorney has made the amendments and arguments to properly frame the issues for appeal. The Applicants make no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

## SUMMARY

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request that this application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckcarter.com.*

The Commissioner is hereby authorized to charge any necessary fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER P.C.

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William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *wmunck@munckcarter.com*